Amendments to the Claims:

This listing of the claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. **(currently amended)** A method for securing a computer system which comprises at least a code interpretation module and memory capacities for storing aan interpreted code having measurable physical imprints ~~provided from said code interpretation module,~~ wherein in order to make more difficult attacks based on physical measurements or requiring synchronization with said interpreted code, the method comprises the steps of:

providing at least two different implementations for at least one instruction of said interpreted code, said different implementations each requiring a different execution time and/or having a different physical imprint while providing an identical result;

selecting one of said different implementations to be executed before each execution of said instruction; and

executing the determined different implementation,~~it consists of introducing at least two types of alternatives in the execution times of the interpreted code, which have an effect on the execution times of the interpreted code or on its measurable physical imprint, said alternatives being introduced according to at least one of the following steps: a first step of causing at certain places of an interpreted code bypasses towards new portions of code which do not belong to the original code in order to complicate the synchronization and the physical imprint of the execution, and/or a second phase of proposing a plurality of implementations of certain instructions, each requiring a different execution time and/or having a different physical~~

~~imprint and providing an identical result, so that two executions of one of said certain instruction within a same code may be performed by two different implementations.~~

2. - 12 **(cancelled)**

13. **(currently amended)** The method according to claim 1, comprising a first mode for introducing a plurality of implementations of certain instructions consisting of enriching the set of instructions recognized by the interpreter with a plurality of implementations for a given instruction~~; the aforesaid instructions are performed either manually by programming or automatically upon code generation~~.

14. **(previously presented)** The method according to claim 1, comprising a second mode for introducing the aforesaid plurality of implementations of certain instructions consisting of comprising in the actual implementation of the instruction, a branching to a portion of at least one alternative code with a variable physical imprint or duration, which dynamically determines the implementation to be executed.

15. **(previously presented)** The method according to claim 14, comprising a first mode for realizing the aforesaid alternative code consisting of proposing a plurality of different implementations of the instruction and by conditioning the choice of the executed version to a dynamical test, i.e., depending on data known at execution.

16. **(cancelled)**

17. **(currently amended)** The method according to claim 14, comprising a ~~third~~ second mode for realizing the aforesaid "alternative code" consisting of improving the aforesaid first ~~and second modes~~ mode for realizing "alternative codes" consisting of replacing the test for deciding on the selected version with a branching in an indirection table containing the addresses of the available version at an index calculated for variable items.

18. **(previously presented)** The method according to claim 1, being implemented on a module for interpreting software code, a so-called virtual machine.

19. **(previously presented)** The method according to claim 18, wherein said virtual machine is a Java platform.

20. **(previously presented)** The method according to claim 1, being implemented on a module for interpreting physical code.

21. **(previously presented)** The method according to claim 1, being implemented on an embedded system and on an interpretation module of the microcontroller or microprocessor type.